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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,079	09/12/2003	Michael W. Morrow	ITL.1028US (P16764)	7093

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EXAMINER	
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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,079	MORROW, MICHAEL W.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/06/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-29 are presented for examination.

2. Claims 22-29 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the relation of the feedback signal to the wireless interface.

3. Regarding claims 1,8,13, the phrase "may" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1 , 8 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 2005/0097552. Although the conflicting claims are not identical, they are not patentably distinct from each other because although the copending claim does not recite the switching to the thread as claimed in the current claim 1 (see also claim 8) , it would have been obvious to one of ordinary skill in the art to use the switching because the copending claim recites the enabling of a execution of non-executing tread, which was recognizable by one of ordinary skill in the art that the enabling could be applied for switching in order to enable the non-executing thread.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1,8,13,17,22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons follow.

5. As to claim 1, no physical transformation can be found in t e claim. Furthermore, no practical application can be found. The step of determining whether execution of instruction may require a long latency is not useful, tangible , and concrete. It is not useful because no specific and substantial application can be found. The language "may" is the step taken to achieve the useful , concrete , and tangible result, but not the final result which is useful, concrete, and tangible. Similarly, the step of switching the thread present no useful, tangible, concrete result. No substantial practical application can be found in this step except the thread switching (see Benson, 409, U.S. at 71-72, 175 USPQ at 676-77). Similar analysis can be done to claims 8,13, and no specific and substantial application can be found in claims 8, 13. As to claims 17,22, providing a feedback to switch the thread , and the feedback signal from a location in processor pipeline has no specific and substantial application. The function of the thread is not being recited in the claim. Therefore, just switching and the feeding back the signal present no substantial practical application. The processor pipeline is not a hardware because it is a pipeline, and a pipeline is an abstract idea, and because no structural element of the computer or the machine pipeline is being recited into the claim. Furthermore, claim 22 recites wireless interface, it raised a doubt what applicant is seeking for protection (see applicant' s specification pages 12,13). It is not sure if the interface is directed to a signal transmission on wireless medium, whci is not tangible.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1-3,8,10,11,17 are rejected under 35 U.S.C. 102(b) as being anticipated by Eickemeyer et al. (6,049,867) .

7. As to claim 1, Eickemeyer taught :

a) determining whether execution of an instruction of a first thread may require a long latency (see the L2/TLB MISS in fig.3, an instruction not explicitly shown but memory access miss should be caused by a R/W instruction, or the like)

b) switching to a second thread the instruction may require the long latency (see the steps of 98 or 100 changing to another thread after the enablement, col.6, lines 25-50).

8. For reason why memory miss caused long latency see col.6, lines 45-50, see also the thread switch due to the miss in col.7, lines 6-56.

9. As to claim 8, Eickemeyer taught switching from a first thread to a second thread if condition that may result stall of a processor pipeline occurs during execution of the first thread processor pipeline (see either the miss condition or the ready condition in fig.3 before changing to another thread or least used thread).

10. As to claims 2,10, Eickemeyer executing at least one additional instruction (see saving the state of thread I or determination of the enable thread in col.6, lines 11-36, saving and enabling were done by implicit command, or the like.) in the first thread while preparing (see determination of ready thread before changing to another thread) to switch to the second thread [another thread or ready thread or the least run thread].

11. AS to claims 3,11, Eickemeyer also included a stochastic analysis (see valid mark) of whether the instruction will result a long latency.

12. AS to claim 17, Eickemeyer taught a processor pipeline having a feedback loop to provide a feedback signal to cause the processor pipeline to switch from a first thread to a second thread (see the feedback loop for change to another thread in fig.4) , the feedback signal to originate from a location in the processor pipeline before instruction execution (for feedback signal, see YES) . The location not explicitly shown, but examiner holds Eickemeyer must have a location in his processor.

13. Claim 1-9, 11-14,16—21 are rejected under 35 U.S.C. 102(b) as being anticipated by Borkenhagen et al. (6,076,157)

14. As to claims 1, 13, Borkenhagen taught (see fig.6) :

a) determining whether execution of an instruction of a first thread may require a long latency (see the first execution attempt of the instruction of thread T0 in 620);

b) switching to a second thread [T1] the instruction may require the long latency (see the switch to a second thread T1 upon no completion of the first instruction in 630, col.16, lines 44-47).

15. For the long latency , see cache miss required a large number of cycle to complete in col.15, lines 44-67, col.16, lines 1-31 for how the number of cycles thrashed.

16. AS to claims 3,11, Borkenhagen also included a stochastic analysis (see cache miss in col.15, lines 43-61) of whether the instruction will result a long latency.

17. AS to claims 4,14, Borkenhagen also taught a lookup table (the control register bit assignment in col.13, lines 29-67, col.4, lines 1-21, see also the comparison of threshold value with the counter col.16, lines 11-37).

18. As to claims 5, 12, 16, 18, 19, 20, Borkenhagen also taught feedback to the fetch unit (see fetch requests for fetch in col.8, lines 50-63). No instruction decoder explicitly shown, but Borkenhagen taught the predetermined conditions for switching could done by hardware and software (see col.12, lines 38-65), therefor, it must have an instruction decoder. See also the instruction unit 220.

19. AS to claim 21, Borkenhagen included list of predetermined conditions (see fig.5).

20. As to claim 6, Borkenhagen also included more than ten cycles (see 30 cycles in col.6, lines 45-52).

As to claim 7, see attempt to switch back , or return to T0 in col.16, lines 47-65.

As to claim 8, Borkenhagen taught a switching from a first thread to a second thread if condition that may result stall of a processor pipeline occurs during execution of the first thread processor pipeline (see the comparison of the threshold before switching thread in col.15, lines 62-67, col.16, lines 1-27) .

21. As to claim 9, Borkenhagen also taught a lookup table (the control register bit assignment in col.13, lines 29-67, col.4, lines 1-21, see also the comparison of threshold value with the counter col.16, lines 11-37).

22. As to claim 17, Borkenhagen taught a processor pipeline having a feedback loop to provide a feedback signal to cause the processor pipeline to switch from a first thread to a second thread (see the feedback loop to return to thread T0 in fig.6) , the feedback signal to originate from a location in the processor pipeline before instruction execution (for feedback signal, see the state signals) .

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 2 , 10 , 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen in view of Chaudhry (2003/0018826)

24. As to claims 2,10, limitations of parent claims have been discussed above. Borkenhagen did not specifically show the executing of at least one additional instruction in the first thread while preparing to switch to the second thread . However,

Chaudhry taught a system allowing continuing execution of a current thread while switching to another thread (see Paragraph [0012]). It would have been obvious to one of ordinary skill in the art to use Chaudhry in Borkenhagen for executing additional instruction while switching a second thread as claimed because the use of Chaudhry could provide Borkenhagen the ability to maintain the processing of the pending thread before the actual thread switch occurred , thereby reducing the time wasted on the switching, and because Borkenhagen also taught an evaluation of the threshold of the thread, no switch would occur if no instruction could be executed (see col.16, lines 18-25), which was a suggestion of the need for continuing the execution of the instructions in the current thread while switching the second thread in order to minimize the latency on the result of the switching , and for doing so, provide a motivation.

25. Claims 22, 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen (6,076,157) in view of Rompaey et al. (5,870,588) .

26. AS to claim 22, Borkenhagen taught a processor pipeline having a feedback loop to provide a feedback signal to cause the processor pipeline to switch from a first thread to a second thread (see the feedback loop to return to thread T0 in fig.6) , the feedback signal to originate from a location in the processor pipeline before instruction execution (for feedback signal, see the state signals) .

Borkenhagen did not specifically teach the wireless interface as claimed. However, Rompaey et al. (5,870,588) taught a wireless network of RISC related processor

(see col.1., lines 18-24 for wireless products, see col.18, lines 31-46 for the RISC processor). It would have been obvious to one of ordinary skill in the art to use Rompaey in Borkenhagen for including he wireless as claimed because the use of Rompaey could expand the Borkenhagen's system capability to adapt to different type of devices, and because Borkenhagen also taught a RISC architecture for supporting unthreaded switching (see col.4, lines 46-67), which was an indication of the applicability of the wireless (taught by Rompaey) into Borkenhagen for providing high performance thread switching, for the above reasons , provided a motivation.

27. As to claims 25-28, Borkenhagen also taught feedback to the fetch unit (see fetch requests for fetch in col.8, lines 50-63). No instruction decoder explicitly shown, but Borkenhagen taught the predetermined conditions for switching could done by hardware and software (see col.12, lines 38-65), therefore, it must have an instruction decoder. See also the instruction unit 220.

28. AS to claim 29, examiner holds that a dipole antenna had been known in the art. Since Rompaey already taught wireless network, one ordinary skill in the art should be able to recognize a dipole antenna could be applied to the wireless network.

29. Claims 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen (6,076,157) in view Rompaey (5,870,588) as applied to claim 22, and further in view of in view of Chaudhry (2003/0018826).

30. As to claims 23, Borkenhagen did not specifically show the executing of at least one additional instruction in the first thread while preparing to switch to the second thread . However, Chaudhry taught a system allowing continuing execution of a current thread while switching to another thread (see Paragraph [0012]). It would have been obvious to one of ordinary skill in the art to use Chaudhry in Borkenhagen for executing additional instruction while switching a second thread as claimed because the use of Chaudhry could provide Borkenhagen the ability to maintain the processing of the pending thread before the actual thread switch occurred , thereby reducing the time wasted on the switching, and because Borkenhagen also taught an evaluation of the threshold of the thread, no switch would occur if no instruction could be executed (see col.16, lines 18-25), which was a suggestion of the need for continuing the execution of the instructions in the current thread while switching the second thread in order to minimize the latency on the result of the switching , and for doing so, provide a motivation.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Nishiyama (6,775,740) is cited for the teaching of continuing the execution of a first thread while preparing the switching to second thread (see col.6, lines 59-67, col.7, lines 1-7).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or

the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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